Attorney Docket No. MP1493-151668
Customer No. 0065589

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:	Examiner: Freshteh N. Aghdam
Daniel Yellin, et al.	Art Unit: 2611
Application No.: 10/734,117	Confirmation No.: 4852
Filed: December 15, 2003	
For: A FILTER FOR A MODULATOR AND METHODS THEREOF	

Mail Stop Amendment
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Declaration of Inventor Pursuant to 37 C.F.R. § 1.131

Sir:

I, Daniel Yellin, hereby declare that:

1. I am a citizen of Israel, which as I was informed by my patent counsel, is a WTO member country. At the time of conceiving and reducing to practice the above identified invention, I was residing in Israel.

2. I am the first named inventor of the subject matter of the above-captioned application, as originally declared in the combined declaration and power of attorney.

3. I was employed by Intel Corporation of Santa Clara, California, the original assignee, during the time the invention was conceived and the patent application was filed.

4. To the best of my recollection and as refreshed by attached **Exhibit A** and **Exhibit B**, the subject invention was conceived on or prior to March 11, 2003.

Exhibit A is a copy of an email dated March 11, 2003 which I sent to my supervisor in Intel to which I attached an "Intel Invention Disclosure Form" which is dated January 1, 2003. **Exhibit B** is a copy of the Intel Invention Disclosure Form that was attached to **Exhibit A**.

6. As seen in **Exhibit A**, I requested my supervisor, Doron Rainish, to approve and forward my patent disclosure. To the best of my recollection my patent disclosure was indeed approved by Mr. Rainish and forwarded to Intel's patent committee as requested, and it was ultimately approved by Intel's patent committee for filing as a patent application.

7. I additionally declare that I worked diligently with my colleagues in Intel and with our outside patent counsel during the period between March 11, 2003, when I sent my email that is shown in **Exhibit A,** and the filing date of the above-captioned application on December 15, 2003, to constructively reduce my invention to practice

I further declare that all statements made herein of my own individual knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified patent application or any patent issued thereon.

Executed by and on the date(s) as set forth below:

By: _____ Date: June 12, 2008

Daniel Yellin, et al.

Exhibit A

Michael Faibisch

From: YELLIN, DANIEL
Sent: Tuesday, March 11, 2003 10:56 AM
To: Rainish, Doron
Cc: Pick, Kobby
Subject: FW: Patent Disclosure

Importance: High

Attachments: Apparatus and Method to Design Digital Pre-Filter for SD Fractional-N Modulator - Disclosure.ZIP

Doron this is the frac-n patent disclosure see below they want you to forward it.
So please approve and follow their guidelines. Thanks, Danny.

Apparatus and Method to Design...

-----Original Message-----
From: Boulden, Janice
Sent: Tuesday, March 11, 2003 12:03 AM
To: Pick, Kobby
Cc: YELLIN, DANIEL
Subject: RE: Patent Disclosure

ALL disclosures must be approved by your manager (must be someone not named as an inventor on the disclosure form). Your manager should forward their approval and the invention disclosure form to the Invention Disclosure Submission email account (one time only). **Do Not "CC" the Invention Disclosure Submission account when sending the IDF to your manager for approval.**

You will need to send this disclosure through your manager for approval.

JB

-----Original Message-----
From: **Pick, Kobby**
Sent: Monday, March 10, 2003 6:21 AM
To: Invention Disclosure Submission
Cc: YELLIN, DANIEL; Pick, Kobby
Subject: Patent Disclosure

Hi

Attached is a patent disclosure of Daniel Yellin and Kobby Pick. << File: Apparatus and Method to Design Digital Pre-Filter for SD Fractional-N Modulator - Disclosure.doc (Compressed) >>

Bye
Kobby Pick

Exhibit B

INTEL INVENTION DISCLOSURE

ATTORNEY-CLIENT PRIVILEGED COMMUNICATION

DATE: 1 January, 2003

It is important to provide accurate and detailed information on this form. The information will be used to evaluate your invention for possible filing as a patent application. When completed and signed, please return this form to the **Legal Department at JF3-147**. If you have any questions, please call **264-0444.**

1.

Inventor: Yellin (Last Name) Daniel (First Name)

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***Corporate Level Group (e.g. iABG, NCG, CEG)** WCCG **Division** PCG **Subdivision** _____

Supervisor* Doron Rainish WWID _____ Phone 972-3-9207229 M/S: _____

Inventor: Pick (Last Name) Kobby (First Name)

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***Corporate Level Group (e.g. iABG, NCG, CEG)** WCCG **Division** PCG **Subdivision** _____

Supervisor* Daniel Yellin WWID 10787418 Phone 972-3-9207187 M/S: _____

***If you are unsure of this information, please discuss with your manager.**

(PROVIDE SAME INFORMATION AS ABOVE FOR EACH ADDITIONAL INVENTOR)

2. Title of Invention: Apparatus and Method to Design Digital Pre-Filter for Sigma-Delta Fractional-N Modulator.

3. What technology/product/process (code name) does it relate to (be specific if you can): 3-Point, Millercreek, Ahwatukee,

4. Include several key words to describe the technology area of the invention in addition to # 3 above: Polar 8PSK/GMSK Modulator, Sigma Delta Converter, Fractional-N PLL

5. Stage of development (i.e. % complete, simulations done, test chips if any, etc.): 70 % complete.

6. (a) Has a description of your invention been, or will it shortly be, published outside Intel:

NO: X YES: _____ If YES, was the manuscript submitted for pre-publication approval? _____

IDENTIFY THE PUBLICATION AND THE DATE PUBLISHED: _____

(b) Has your invention been used/sold or planned to be used/sold by Intel or others?

NO: _____ YES: X DATE WAS OR WILL BE SOLD: According to 3-Point, Millercreek, Ahwatukee schedules

(c) Does this invention relate to technology that is or will be covered by a SIG (special interest group)/standard/ or specification?

NO: ___X___ YES: _____ Name of SIG/Standard/Specification: _____

(d) If the invention is embodied in a semiconductor device, actual or anticipated date of tapeout? According to 3-Point, Millercreek, Ahwattukee schedules _____

(e) If the invention is software, actual or anticipated date of any beta tests outside Intel _____

7. Was the invention conceived or constructed in collaboration with anyone other than an Intel blue badge employee or in performance of a project involving entities other than Intel, e.g. government, other companies, universities or consortia? NO: X YES: _____ Name of individual or entity: _____

8. Is this invention related to any other invention disclosure that you have recently submitted? If so, please give the title and inventors: 1.)_____ 2.) _____

****

References

[S1] M. H. Perrot and M. D. Trott, "A Modeling Approach for Σ-Δ Fractional-N Frequency Synthesizers Allowing Straightforward Noise Analysis", *IEEE Journal of Solid-State Circuits*, Vol. 37, pp 1028-1038 ,August 2002.

[S2] Patent 6,008,703: M.H. Perrott, "Digital Compensation for Wideband Modulation of Phase-Locked-Loop Frequency Synthesizer".

Background

Fractional N sigma-delta modulation is gaining significant interest in the cellular industry as this is a very cost-effective architecture for the transmission path of digitally modulated signals. In fact, all future GSM/GPRS/EDGE chipsets that we investigated employ this technology (3 different vendors)! The key idea is to employ polar modulation, i.e. to separate the signal into its instantaneous amplitude and phase/frequency components (rather than to the classical I & Q components), and modulate these components independently. While the amplitude path uses some sort of plain AM modulation technique, the phase path uses the PLL as the phase modulator. As explained in [S1]-[S2] , the key difficulty with this approach is that the PLL bandwidth must be quite small to allow reasonable operation, much smaller than the actual bandwidth of the Tx signal's instantaneous phase/frequency. Therefore, the solution proposed in [S2] is to use a pre-emphasis filter that will emphasize those frequency components that would be attenuated by the PLL. This pre-emphasis filter turns out to be a key aspect in the design of this Tx path, yet the proposal in [S2 – e.g. Column 10 lines 6-21] **Error! Reference source not found.** is to employ inverse filtering to the linearized response of the PLL. In this disclosure we address methods and apparatus to design this pre-emphasis better, and possibly to adjust it adaptively. Our approach provides the following advantages:

- Implementation complexity – inverse filtering yields a high-order IIR which suffers from stability problems - whereas with our approach we are able to utilize an FIR which is always stable! and often can be operated at much lower sampling rates and with fewer bits (i.e. smaller word length) .
- Calibration mechanisms – conventional practice requires calibration mechanisms in order to very accurately calibrate the PLL to the pre-defined pre-emphasis filters, whereas with our approach it is possible to avoid these calibration mechanisms and adjust the digital pre-filter to match the analog PLL (and not vise-versa). This is impossible to achieve with the conventional practice because of the need to guarantee stability of the IIR pre-filter (without calibration, some PLL's will simply not generate stable inverse filters).
- FIR pre-filtering lends itself naturally into an adaptive mechanism that can be used to track voltage/tempretaure/aging, etc, variations of the PLL, and again simplify and improve the design.
- Rather than just invert the PLL's transfer function, with our approach it is possible to take the PLL impairments (e.g. phase noises) into account and design the pre-filter (we may choose to design either an FIR or an IIR) under various optimization criteria (e.g. spectral cleanliness at the output) – thus with our approach it is possible to better tolerate the different PLL impairments.

General Description

A general block diagram of the system is presented in Figure 1:

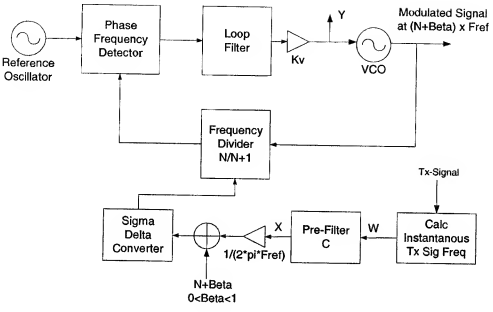

Figure 1: Fractional-N SD Modulator Block Diagram

As explained above, this patent application is about designing the pre-filter "C". In order that the instantaneous signal (w), be transferred to the VCO input (y) with minimal distortion, the overall response from w to y should be close to flat. In order to decide what is the optimal pre-filter to use, one often takes the following steps:

1. Build a linear model for the PLL of Figure 1 (e.g. according to [1]), and calculate the transfer function from x to y in Figure 1. Denote this transfer function by H{w}.
2. Design a pre-filter such that the overall response from w to y will be flat in the desired frequency range, and low pass in nature above those frequencies (the reason for the low-pass nature is for the purpose of attenuating the quantization noise generated by the Sigma-Delta block).

The conventional practice is simply to choose

$$C(w) = H(w)^{-1}$$

which yields a complex IIR filter and often requires adding poles/zeros to C(w) to guarantee its low-pass nature above a certain frequency (there is no point to invert the PLL response in those region where there is no significant frequency component of the Tx signal) and/or to stabilize C(w) [S2]. Note that this inverse filtering is quite problematic, as H(w) is very narrow-band, hence its inverse is a filter with extremely large gain.

Batch (off-line) processing

Our proposal for off-line processing composes of the following steps.

1. Build a linear model for the PLL (e.g. according to [S1]).
2. Add the various impairments, e.g. phase noises, of the different PLL components (Optional step).
3. Decide on a topology for C (e.g. an FIR of order p, an IIR of orders (p,q), etc).
4. Calculate C(w) to minimize a pre-defined cost-function so that the overall cost is minimized, i.e.

$$C(w) = ArgMin_{C(w)}\{Cost(W,Y)\}$$

In one embodiment, the cost could be the mean square error (MSE), i.e.

$$Cost(W,Y) = E\{|W(t) - Y(t)|^2\}$$

or a weighted MSE in the frequency domain (e.g. to give more weight to those frequencies where spectral cleanliness is more important),

$$Cost(W,Y) = E\{ \int_{-\infty}^{\infty} P(w) \, |W(w) - Y(w)|^2 \, dw \}$$

where P(w) is a user-defined, positive, weight function.
It should be noted that these particular costs can be easily minimized using equalization theory, as is detailed in the Appendix. In other embodiments, other cost functions may be utilized e.g. those that measure spectral cleanliness of the overall Tx signal. We note that for the particular MSE cost functions, Step 2 above is redundant when all impairments can be represented as additive noise terms, as different choices of C(w) will not affect that total contribution of these additive impairments to the MSE or weighted MSE cost.

If the pre-filter is chosen to be an FIR, then it avoids all stability problems (that are encountered with an IIR implementation) that often also influence the fixed-point arithmetic involved (i.e. FIR often requires fewer bits).
Also, since we can easily re-calculate the FIR per any value of the PLL parameters (and its stability is guaranteed), it may avoid the need for calibration mechanisms, while with the IIR approach it is common that people need to "hand-craft" an IIR to a specific setting [S2] – hence the PLL should be calibrated to that specific setting.

Adaptive (on-line) processing

There are numerous approaches that can be followed here, they all require some sort of feedback from the VCO input, output (or further away e.g. the antenna) to close the loop. Then, a variety of methods similar to adaptive equalization techniques could be employed. Below is one preferred embodiment. As can be seen, the VCO input and the

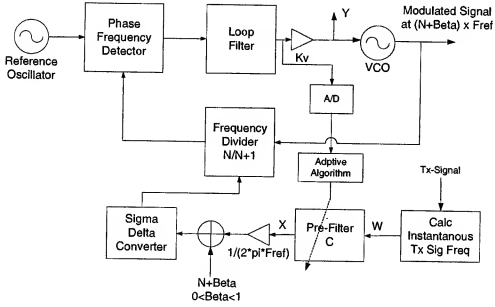

Figure 2: Adaptive Pre-Filtering approach - one embodiment

As can be seen, the input to the pre-emphasis filter is compared to the VCO input (after digitization), and accordingly the pre-filter is adapted. Thus, any impairments, offsets, drifts, etc of the analog portion of the PLL would drive the pre-filter values to that setting value that minimizes the pre-specified adaptive mechanism cost function (again an MSE cost could be one option). Hence potentially avoiding the need for complex analog measurement & calibration mechanisms, as any variations would be compensated for by the adaptive algorithm.

Appendix

Linear Model for the System

We will make the linear approximation to the system in the phase domain. The system include several elements that are non-linear:

1. Phase detector.
2. Frequency divider.

- The phase detector could be approximated for small phase differences (when the loop is "locked"), simply by the phase difference between the reference signal and the divider output.
- The frequency divider linear model could be derived using the following steps:
  - The division x(t)/N(t) could be broken by the Taylor serious approximation into:
    - X(t)/(Nnominal+dN(t))=~x(t)/Nnominal(1-dN(t)) which replaces division by multiplication.
  - Further approximation could be made to achieve full linearization.

The result full linear model of Figure 1 is presented in the following figure:

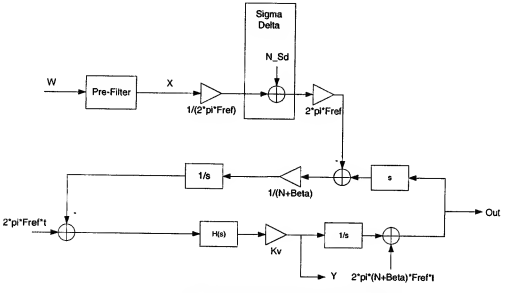

Figure 3: Linearized PLL Block Diagram

The transfer function from x to y is:

$$\frac{Y(s)}{X(s)}=\frac{(K_v/N)\cdot H(s)/s}{1+(K_v/N)\cdot H(s)/s}$$

Equation 1

Pre-Filter Design

In order that no significant frequency and phase distortion will occur, the overall transfer function from w to y should be of 0 dB gain up to frequency f_0, and linear phase in that range. In order for the above condition to happen, we need that transfer function from w to x up to f_0 to be:

$$\frac{X(s)}{W(s)}=\frac{1+(K_v/N)\cdot H(s)/s}{(K_v/N)\cdot H(s)/s},\ s=j\cdot 2\cdot\pi\cdot f,\ f<f_0$$

Equation 2

If we implement is in a straightforward manner as the inverse IIR to Y(s)/X(s), we will run into the following problems:

- The inverse IIR forces adding zeros and poles in order to stabilize the pre-filter.
- The pre-filter frequency response at frequencies above f_0 should have low pass nature, and should decline as fast as possible in order not to force the Sigma Delta to be in saturation, and not to increase the quantization noise, as a result of that, additional poles or filter that will attenuate the frequencies above f_0.

- The order of the pre-filter could not be a design parameter, but should have a one to one relation to the order of the closed loop transfer function.
- Another aspect of the problem is that we want to reduce the sampling rate of the pre-filter as much as possible from current consumption aspects.

As a result from the above reasons we applied a FIR MMSE equalizer, that its fundamentals are taken from the communication theory. We will now derive the MMSE equalizer for the above problem. The system model is described is the following figure:

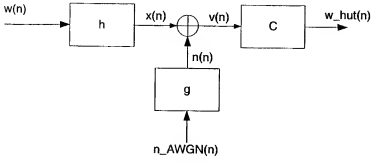

Figure 4: Equalizer Block Diagram

Where:
w – the input signal.
w_hut – the restored input signal.
h – is the impulse response of STF(z)
STF(z) = Y(z)/X(z) as the Bi-Linear transform of Y(s)/X(s)
n_AWGN – is additive white Gaussian noise.
g – is the shaping filter of the noise.
c – the desired equalizer FIR filter.

Our aim is to find a FIR filter C, that will minimize the mean square error that is defined as:
$e \equiv w(n) - \hat{w}(n)$

Equation 3

Where:

$$\hat{w}(n) = \overline{C}^{H} \cdot \overline{V}$$

$$\overline{V} = H \cdot \overline{W} + \overline{N}$$

$$H = \begin{bmatrix} h(M+L) & \cdot & h(L) & \cdot & h(-M+L) \\ \cdot & & \cdot & & \cdot \\ h(M) & & h(0) & & h(-M) \\ \cdot & & & & \cdot \\ h(M-L) & \cdot & h(n-(L-1)) & \cdot & h(-M-L) \end{bmatrix}_{[(2\cdot L+1)\times(2\cdot M+1)]}$$

$$\overline{W} = \begin{bmatrix} w(n-M) \\ \cdot \\ w(n) \\ \\ w(n+M) \end{bmatrix}_{[(2\cdot M+1)\times 1]}$$

$$\overline{N} = \begin{bmatrix} n(n+L) \\ \cdot \\ n(n) \\ \\ n(n-L) \end{bmatrix}_{[(2\cdot L+1)\times 1]}$$

Equation 4

Where:
2xM+1 – is assumed to be the impulse response of STF(z) length.
2xL+1 – is assumed to be the equalizer length.
N – is the AWGN noise after passing it through filter g. g is selected to be a high pass filter with cutoff above f_0, so that the equalizer response at high frequencies will be attenuated.
We make the following assumptions:

1. From the no correlation between the error and the observations: $E\{e(n)\cdot \overline{V}^H\}=\overline{0}^H$.
2. $E\{w(n)\cdot n(n+k)^*\}=0, \forall k$
3. $E\{w(n)\cdot w(n+k)^*\}=\begin{cases}\sigma_w^2, k=0\\ 0, k\neq 0\end{cases}$
4. $E\{n(n)\cdot n(n+k)^*\}=\begin{cases}\sigma_n^2, k=0\\ 0, k\neq 0\end{cases}$

From assumption 1 it follows that:
$E\{w(n)\cdot \overline{V}^H\}=E\{\hat{w}(n)\cdot \overline{V}^H\}$

Equation 5

After substitution of Equation 4 into Equation 5 we get:
$E\{\hat{w}(n)\cdot \overline{V}^H\}=\overline{C}^H\cdot E\{\overline{V}\cdot \overline{V}^H\}=\overline{C}^H\cdot E\{(H\cdot \overline{V}+\overline{N})\cdot(\overline{V}^H\cdot H^H+\overline{N}^H)\}=$
$=\overline{C}^H\cdot\left[E\{H\cdot \overline{V}\cdot \overline{V}^H\cdot H^H\}+E\{\overline{N}\cdot \overline{N}^H\}\right]=\overline{C}^H\cdot\left[H\cdot H^H\cdot\sigma_w^2+G\cdot G^H\cdot\sigma_n^2\right]$
$\sigma_w^2=E\{|w(n)|^2\}$
$\sigma_n^2=E\{|n_{AWGN}(n)|^2\}$

Equation 6

Where:
G is defined in a similar manner to H with g.
$E\{w(n)\cdot \overline{V}^H\}=\sigma_w^2\cdot[h(L)\quad .\quad h(0)\quad .\quad h(-L)]$

Equation 7

From Equation 6 Equation 7 and Equation 5, and after applying the Hermit operator we get the MMSE solution to be:

$$\overline{C}=R_{vv}^{-1}\cdot\overline{R}_{vw}=\left[H\cdot H^H\cdot\sigma_w^2+G\cdot G^H\cdot\sigma_n^2\right]^{-1}\cdot\begin{bmatrix}h(L)\\ .\\ h(0)\\ .\\ h(-L)\end{bmatrix}\cdot\sigma_w^2$$

Equation 8

Note that it is also possible to calculate c empirically.

One Possible Embodiment

One possible embodiment of the invention is as 8PSK / GMSK modulator for the Edge standard. Figure 5 presents a polar modulation loop that employ Fractional-N Sigma Delta modulator at the phase path. The symbols generator generates the baseband Edge symbols. The Amplitude Phase Splitter, splits the baseband symbols to amplitude and phase paths. The phase path symbols are differentiated to produce the frequency symbols. The frequency symbols are divided by the reference frequency to produce the desired division ratio of the instantaneous frequency. The instantaneous frequency division ratio is passed through the pre-filter, and then to the Sigma Delta converter. The output of the sigma delta is added to the carrier division ratio and passed ad the division ratio serious to the PLL. The Fractional-N PLL modulates the phase to carrier frequency. The phase at the carrier frequency is fed into the PA that its gain is controlled by the output from the phase path, to produce the RF signal.

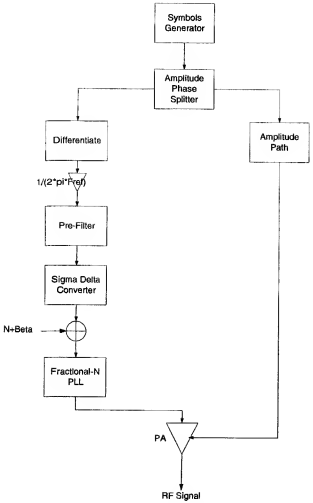

Figure 5: Polar Modulator for Edge Block Diagram

Components

The invention includes the following components (relates to Figure 1, Figure 3 and Figure 4):

- Linearized PLL model.
- PLL closed loop transfer function.
- Noise shaping filter.
- MMSE equalizer.

Linearized PLL Model

The linearized PLL model is described in detail in the section Linear Model for the System, and in Figure 3. In general it used to calculate the PLL closed loop transfer function that will enable calculating the desired pre-filter.

PLL Closed Loop Transfer Function

The PLL closed loop transfer function calculation is described in details in the section Linear Model for the System, and in Figure 3. In general it used to calculate the desired pre-filter that will cause the overall response of the instantaneous frequency to be flat in the desired range of frequencies.

Noise Shaping Filter

The noise shaping filter is described in detail in the section Pre-Filter Design and in Figure 4. In general it used to shape a high pass noise for frequencies above f_0, so that the MMSE equalizer response will be flat for frequencies below f_0 and low pass in nature for frequencies above f_0.

MMSE Equalizer

The MMSE equalizer is described in detail in the section Pre-Filter Design and in Figure 4. In general it used to design a FIR filter that will cause the overall response to be flat for frequencies below f_0 and low pass in nature for frequencies above f_0.

DATE: _____ SUPERVISOR: _____

BY THIS SIGNING, I (SUPERVISOR) ACKNOWLEDGE THAT I HAVE READ AND UNDERSTAND THIS DISCLOSURE, AND RECOMMEND THAT THE HONORARIUM BE PAID